ABSTRACT OF THE DISCLOSURE

A semiconductor layer with a threshold voltage for n-channel is formed and patterned to TFT island areas. A gate insulating film is deposited. The first gate electrode layer is fomed and pattered to form an opening. Phosphorous ions are implanted into a p-channel TFT in the opening to set threshold voltage for p-channel TFT. A second gate electrode layer is formed and patterned to form second gate electrodes. By using the first gate electrode layer as a mask, boron ions are implanted at a high concentration to form source/drain regions of the p-channel TFT. By using the second gate electrodes as a mask, the first gate electrode layer is etched to form gate electrodes. Phosphorous ions are implanted at a low concentration to form LDD regions. By using a fourth mask, P ions are implanted at a high concentration to form source/drain regions of n-channel TFTs.